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Call for Papers

MCHPC'22: Workshop on Memory Centric High Performance Computing
held in conjunction with SC22: The International Conference on High Performance Computing, Networking, Storage and Analysis and in cooperation with IEEE Computer Society

Time/Date: 2:00PM - 5:30PM, U.S. Central Standard Time, Sunday, November 13, 2022
Location: Room D222

https://passlab.github.io/mchpc/mchpc2022

Submission Deadline: August 19, 2022

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The growing disparity between CPU speed and memory speed, known as the memory wall problem, has been one of the most critical and long-standing challenges in the computing industry. The situation is further complicated by the recent expansion of the memory hierarchy and the blurred boundary between memory and storage. The memory hierarchy is becoming deeper and more diversified with the adoption of new memory technologies and architectures, including 3D-stacked memory, non-volatile random-access memory (NVRAM), memristor, hybrid software and hardware caches, etc. Computer architecture and hardware systems, operating systems, storage and file systems, programming stack, performance models and tools are being enhanced, augmented, or even redesigned to address the performance, programmability, and energy efficiency challenges of the increasingly complex and heterogeneous memory systems for HPC and data-intensive applications.

The MCHPC workshop aims to bring together computer and computational science researchers, from industry, government labs and academia, concerned with the challenges of efficiently using existing and emerging memory systems. The term performance for memory systems is general, which includes latency, bandwidth, power consumption and reliability from the aspect of hardware memory technologies to what it is manifested in the application performance. The topics of interest for the MCHPC workshop include, but are not limited to:

- Software, hardware, and co-design approaches that ease the adoption and optimize the use of processing-in-memory and near-memory computing technologies.
- Evaluation, characterization, performance analysis, and use cases of emerging memory technologies, including non-volatile memories, high-bandwidth memory, heterogeneous memory, disaggregated memory, etc.
- Programming interfaces or language extensions that improve the programmability of using emerging memory technologies and systems, heterogeneous memory system and multi-dimensional data, and unified memory systems.
- Compiler, runtime, and system techniques for optimizing data layout and placement, page migration, coherence and consistency enforcement, latency hiding and improving bandwidth utilization and energy consumption of heterogeneous memory systems.
- Enhancement or new development for operating systems, storage and file systems, and I/O system that address challenges of existing and emerging memory technologies, heterogeneous memory systems, and the blurred boundary between memory and storage.
- Tools, modeling, evaluation, and case study of memory system behavior and application performance that reveals the limitation and characteristics of existing memory systems.
- Application development and optimization for new memory architecture and technologies.

Important Dates

- Submission Deadline -- August 19, 2022
- Notifications -- September 9, 2022

- Camera Ready Papers -- October 9, 2022, including IEEE Copyright Form
- November 13 afternoon, 2022 – Workshop

Submission

Authors are invited to submit manuscripts in English structured as technical papers up to 8 pages or as short papers up to 5 pages, both of letter size (8.5in x 11in) and including figures, tables, and references. Submissions not conforming to these guidelines may be returned without review. Your paper should be formatted using IEEE conference format which can be found from https://www.ieee.org/conferences/publishing/templates.html. The workshop encourages submitters to include reproducibility information, using Reproducibility Initiative for SC'22 Technical Papers as guideline.

All manuscripts will be peer-reviewed and judged on correctness, originality, technical strength, and significance, quality of presentation, and interest and relevance to the workshop attendees. Submitted papers must represent original unpublished research that is not currently under review for any other conference or journal. Papers not following these guidelines will be rejected without review and further action may be taken, including (but not limited to) notifications sent to the heads of the institutions of the authors and sponsors of the conference. Submissions received after the due date, exceeding length limit, or not appropriately structured may also not be considered. At least one author of an accepted paper must register for and attend the workshop. Authors may contact the workshop organizers for more information.

Papers should be submitted electronically at: https://submissions.supercomputing.org/, choose "SC22 Workshop: MCHPC'22: Workshop on Memory Centric High Performance Computing". The final papers are planned to be published through IEEE Computer Society. Published proceedings will be included in the IEEE Xplore digital library.

Organizers

- Ron Brightwell (Sandia National Laboratory, rbbrigh@sandia.gov)
- Maya B Gokhale (Lawrence Livermore National Laboratory, gokhale2@llnl.gov)
- Yonghong Yan (University of North Carolina at Charlotte, yyan7@uncc.edu)
- Ivy B. Peng (KTH Royal Institute of Technology, ipeng@acm.org)

Steering Committee

- Xian-He Sun (Illinois Institute of Technology)
- Yonghong Yan (University of North Carolina at Charlotte)
- Ron Brightwell (Sandia National Laboratory)
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