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Call for Papers

MCHPC'21: Workshop on Memory Centric High Performance Computing
held in conjunction with SC21: The International Conference on High Performance Computing, Networking, Storage and Analysis and in cooperation with IEEE TCHPC

Time/Date: 9:00AM - 5:30PM, U.S. Central Standard Time, Sunday, November 14, 202
Location: America's Center, St. Louis, MO

https://passlab.github.io/mchpc/mchpc2021

Submission Deadline: September 2nd, 2021

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The growing disparity between CPU speed and memory speed, known as the memory wall problem, has been one of the most critical and long-standing challenges in the computing industry. The situation is further complicated by the recent expansion of the memory hierarchy, which is becoming deeper and more diversified with the adoption of new memory technologies and architectures including 3D-stacked memory, non-volatile random-access memory (NVRAM), memristor, hybrid software and hardware caches, etc. Computer architecture and hardware system, operating systems, storage and file systems, programming stack, performance model and tools are being enhanced, augmented, or even redesigned to address the performance, programmability and energy efficiency challenges of the increasingly complex and heterogeneous memory systems for HPC and data-intensive applications.

The MCHPC workshop aims to bring together computer and computational science researchers, from industry, government labs and academia, concerned with the challenges of efficiently using existing and emerging memory systems for high performance computing. The term performance for memory system is general, which include latency, bandwidth, power consumption and reliability from the aspect of hardware memory technologies to what is manifested in the application performance. The topics of interest for the MCHPC workshop include, but are not limited to:

- The challenges and software and hardware solutions of using 3-D stack memory, NVDIMM, memristor and other processor/compute-in-memory technology.
- Programming interfaces or language extensions that improve the programmability of using emerging memory technologies and systems.
- Compiler and runtime techniques for optimizing data layout, movement and consistency enforcement for latency hiding and for improving bandwidth utilization and energy consumption of memory systems.
- Enhancement or new development for operating systems, storage and file systems, and I/O system that address existing and emerging memory systems.
- Modeling, evaluation, and case study of memory system behavior and application performance that reveals the limitations and characteristics of existing memory systems.
- Application development and optimization for memory architecture and technologies.

Important Dates

- Submission Deadline -- September 2nd, 2021
- Notifications -- September 24 2021
- Camera Ready Papers -- October 10 2021, IEEE Copyright Form due by October 6
- November 14th 2021 – Workshop

Submission

Authors are invited to submit manuscripts in English structured as technical papers up to 8 pages or as short papers up to 5 pages, both of letter size (8.5in x 11in) and including figures, tables, and references. Submissions not conforming to these guidelines may be returned without review. Your paper should be formatted using IEEE conference format which can be found from https://www.ieee.org/conferences/publishing/templates.html. The workshop encourages submitters to include reproducibility information, using Reproducibility Initiative for SC'21 Technical Papers as guideline.

All manuscripts will be peer-reviewed and judged on correctness, originality, technical strength, and significance, quality of presentation, and interest and relevance to the workshop attendees. Submitted papers must represent original unpublished research that is not currently under review for any other conference or journal. Papers not following these guidelines will be rejected without review and further action may be taken, including (but not limited to) notifications sent to the heads of the institutions of the authors and sponsors of the conference. Submissions received after the due date, exceeding length limit, or not appropriately structured may also not be considered. At least one author of an accepted paper must register for and attend the workshop. Authors may contact the workshop organizers for more information.

Papers should be submitted electronically at: https://submissions.supercomputing.org/, choose "SC21 Workshop: MCHPC'21: Workshop on Memory Centric High Performance Computing". The final papers are planned to be published through IEEE TCHPC. Published proceedings will be included in the IEEE Xplore digital library.

Organizers

- Yonghong Yan (University of North Carolina at Charlotte, yyan7@uncc.edu)
- Ron Brightwell (Sandia National Laboratory, rbbrigh@sandia.gov)
- Xian-He Sun (Illinois Institute of Technology, sun@iit.edu)
- Maya B Gokhale (Lawrence Livermore National Laboratory, gokhale2@llnl.gov)

Program Committee

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- Mingyu Chen (Chinese Academy of Sciences)
- Tom Deakin (University of Bristol)
- Clea Marples (Lawrence Livermore National Laboratory)
- Kyle Hale (Illinois Institute of Technology)
- Seyong Lee (Oak Ridge National Laboratory)
- Stephen L Olivier (Sandia National Laboratories)
- Dong Li (University of California, Merced)
- Ivy B. Peng (Lawrence Livermore National Laboratory)
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