CSCE 513 Computer Architecture Fall 2018

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Course information

- **Meeting Time:** 8:05 9:20 AM Monday Wednesday
- Place: 2A31, Swearingen Engineer Center
- Grade: 50% for 5 assignments, 20% midterm, and 30% final exam
- Instructor: Yonghong Yan
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 - Office: Room 2211, Storey Innovation Center (Horizon II), 550 Assembly St, Columbia, SC 29201
 - Tel: 803-777-7361
 - Office Hours: Monday 9:20 10:20 AM in classroom or my office, or Tuesday 10:00 - 11:00 AM my office, or by appointment
- **Public Course website**: http://passlab.github.io/CSCE513
- Private and assignment submission: https://dropbox.cse.sc.edu/
- Website syllabus for more details

Exams and Online Broadcasting

- Exams (50%): Test Fundamentals, close book/notes
 - Midterm (20%, October 15, Monday during class)
 - Final Exam (30%, December 12, Wednesday, 9:00 11:30 AM)
 - One page note sheet
- Graduate vs undergraduate
 - Extra questions for graduate in assignments and exams
 - Undergraduate earn bonus points of those questions
- Broadcasting
 - From <u>https://webconnect.sc.edu/csce513/</u>
 - Check details:

https://passlab.github.io/CSCE513/OnlineAdobeConnect.html

Required Textbook (CAQA)

- Computer Architecture A Quantitative Approach, 6th Edition 2017
 - John L. Hennessy and David A. Patterson



Reference Textbook (COD)

- Computer Organization and Design, RISC-V Edition: The Hardware/Software Interface, 2017
 - John L. Hennessy and David A. Patterson
 - Introductory book



Authors of the Textbook

John L. Hennessy and David A. Patterson

Pioneers of Modern Computer Architecture Receive ACM A.M.

Turing Award

Hennessy and Patterson's Foundational Contributions to Today's Microprocessors Helped Usher in Mobile and IoT Revolutions

NEW YORK, NY, March 21, 2018 – ACM C, the Association for Computing Machinery, today named John L. Hennessy C, former President of Stanford University, and David A. Patterson C, retired Professor of the University of California, Berkeley, recipients of the 2017 ACM A.M. Turing Award for pioneering a



• Proach to the design and evaluation of computer architectures with enduring or industry. Hennessy and Patterson created a systematic and quantitative r, lower power, and reduced instruction set computer (RISC) microprocessors. and repeatable principles that generations of architects have used for many dustry. Today, 99% of the more than 16 billion microprocessors produced rs, and are found in nearly all smartphones, tablets, and the billions of prise the Internet of Things (IoT).

https://www.acm.org/media-center/2018/march/turing-award-2017

Dr. Jason D. Bakos wrote chapters/exercises as well

CAQA Textbook Chapter Order for the Lecture

- Chapter 1:
 - Introduction and Fundamentals of Quantitative Design and Analysis
- Appendix A:
 - Instruction Set Principles
- Appendix C:
 - Pipelining: Basic and Intermediate Concepts
- Appendix B:
 - Review of Memory Hierarchy
- Midterm (Oct 15th)

Read at least 15 pages per week in average following the class schedule.

- Chapter 2:
 - Memory Hierarchy Design
- Chapter 3:
 - Instruction-Level Parallelism and Its Exploitation
- Chapter 4:
 - Data-Level Parallelism in Vector, SIMD, and GPU Architectures
- Chapter 5:
 - Thread-Level Parallelism
- Chapter 7:
 - Domain Specific Architectures
- Final (Dec 12th)

Refer to COD book if needed